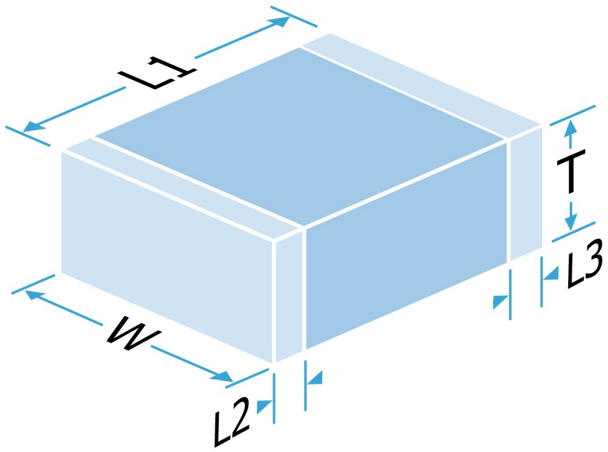
# Multilayer Ceramic Chip Capacitor

| | |
|---|---|
| **Part Number:** 1812Y1000105KET | **Description:** 1812 100Vdc 1.0uF ±10% X7R (2R1) to AEC-Q200 (CTI ≥ 600) |

A range of X7R MLC capacitors fully tested and approved to automotive specification AEC-Q200. Available in a wide selection of chip sizes, working voltages and termination options, including FlexiCap™, the world's first commercially available flexible termination.

DR1, WR2 and WR3 parts have a voltage de-rating above 105°C.

WS2, WS3, WR2 and WR3 parts use StackiCap™ patented construction technology.




## Mechanical Specification

| | |
|---|---|
| Size Code | 1812 |
| Length (L1) in mm (") | 4.5 +0.40/-0.30 (0.180 +0.016/-0.012) |
| Width (W) in mm (") | 3.2 ± 0.20 (0.126 ± 0.008) |
| Thickness (T) in mm (") | 2.5 Max (0.1 Max) |
| Minimum Termination Band (L2,L3) in mm (") | 0.25 (0.010) |
| Maximum Termination Band (L2,L3) in mm (") | 1.143 (0.045) |
| Termination Material | FlexiCap™ Polymer termination, Nickel barrier, Sn Plated Solder (RoHS compliant) |
| Solderability | IEC-60068-2-58 |
| Packaging | 7" Reel Horizontal Orientation, 500 per reel |
| Conformal Coating | Not normally required |

## General Electrical Specification

| | |
|---|---|
| Rated Voltage | 100Vdc |
| Nominal Capacitance Value | 1.0uF |
| Capacitance Tolerance | ±10% |
| Tangent of Loss Angle (Tan δ) | ≤0.025 |
| Capacitance and Tan δ Test Conditions | 1.0Vrms @ 1kHz |
| Voltage Proof (Voltage applied for 5 secs max. @ 50mA max. charge current. 50% Max, RH) | 250Vdc |
| Min Insulation Resistance (IR) | 1.00GOhm @ 100Vdc |
| Dielectric Classification | X7R (2R1) to AEC-Q200 (CTI ≥ 600) |
| Rated Temperature Range | -55°C / +125°C |
| Maximum Capacitance Change over Temperature Range | No DC Voltage ±15%<br>Rated DC Voltage - |
| Climatic Category (IEC) | 55/125/56 |
| Ageing Characteristic | <2% per decade (nominal capacitance is 1000 hour value) |

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Europe: KPD-Europe-sales@knowles.com
Asia: KPD-Asia-sales@knowles.com
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|---|---|
| **Part Number:** 1812Y1000105KET | **Description:** 1812 100Vdc 1.0uF ±10% X7R (2R1) to AEC-Q200 (CTI ≥ 600) |

## Environmental

| | |
|---|---|
| RoHS Compliant to 2011/65/EC as amended by 2015/863/EU | Compliant |
| REACH Compliant | 250 compliant |
| California Proposition 65 | No exposure risk |

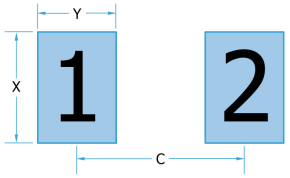
## Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover, especially under high humidity conditions. Board cleanliness and environmental conditions can also impact this. Refer to application note AN0043 for further information.

IPC-7351 pad design

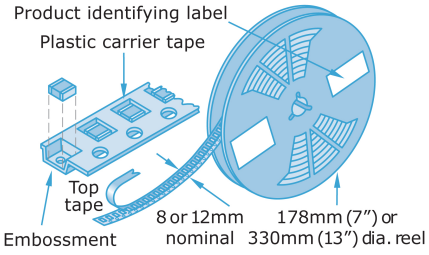
| | 1812 | |
|---|---|---|
| C | 4.00mm | 0.157" |
| Y | 1.55mm | 0.061" |
| X | 3.40mm | 0.134" |




## Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



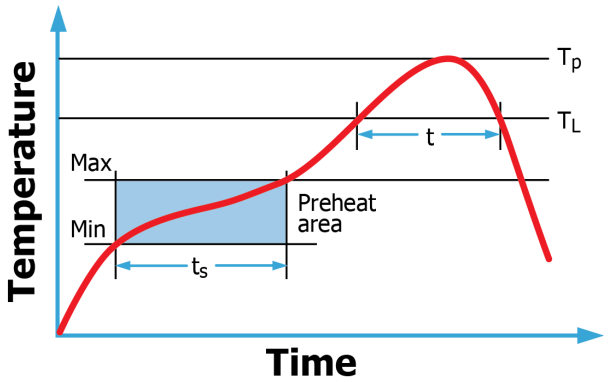

## Soldering

Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.




Application notes with mounting and handling guidance are available on request.

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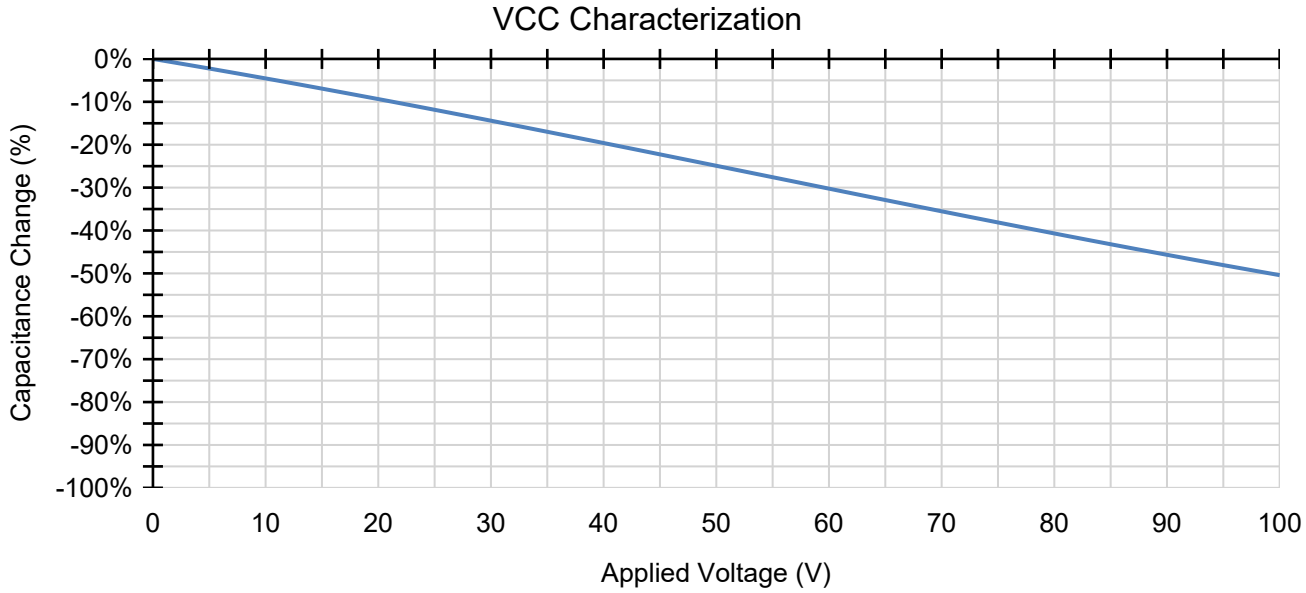
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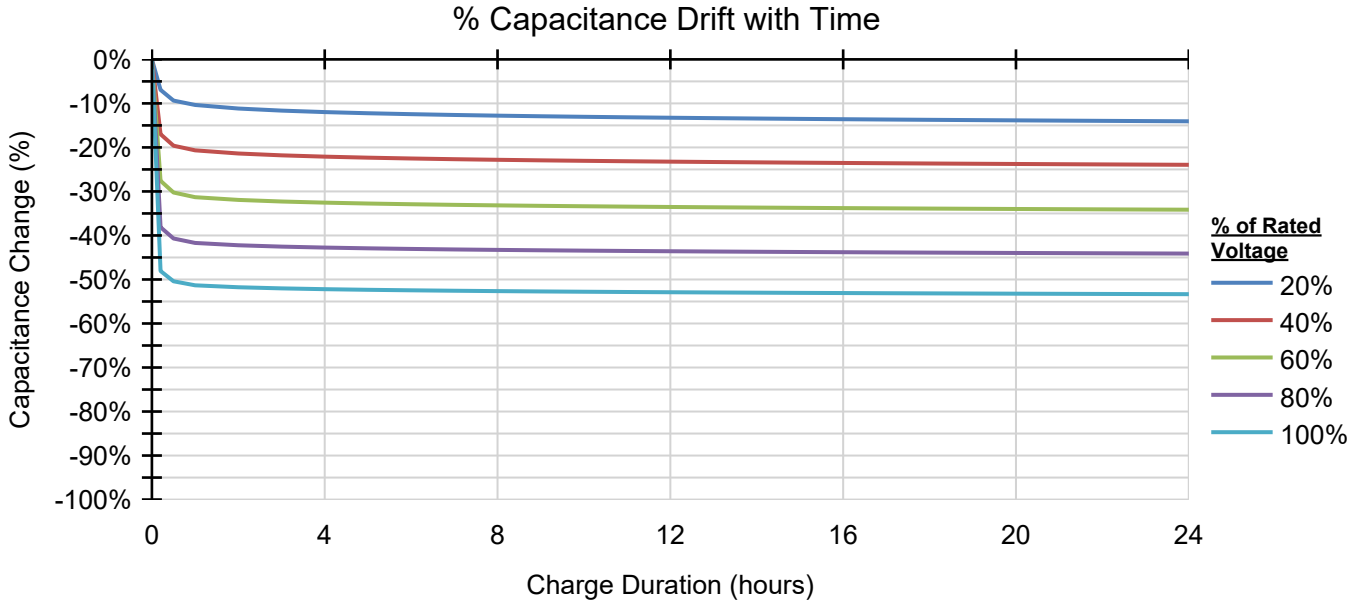
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# Multilayer Ceramic Chip Capacitor

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|---|---|
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## DC Bias Characteristics




The curves represent the 'typical worst case' curve – i.e. the typical curve of a 'worst case' component having the most capacitance loss delivered against the specification.

Knowles Precision Devices reserve the right to substitute any component with a similar component of the same or higher specification. In some cases this may mean that the capacitance drop with applied voltage is, in practice, less than the curve shown

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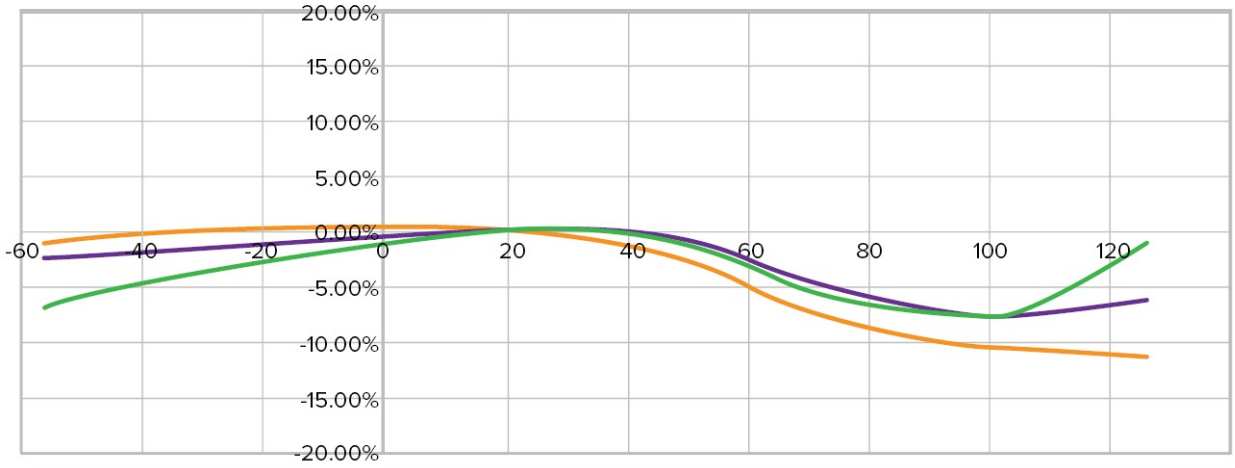
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# Multilayer Ceramic Chip Capacitor

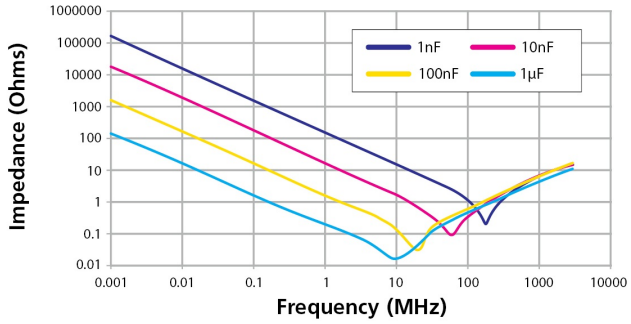
| | |
|---|---|
| **Part Number:** 1812Y1000105KET | **Description:** 1812 100Vdc 1.0uF ±10% X7R (2R1) to AEC-Q200 (CTI ≥ 600) |

## Typical Capacitance Change vs Temperature

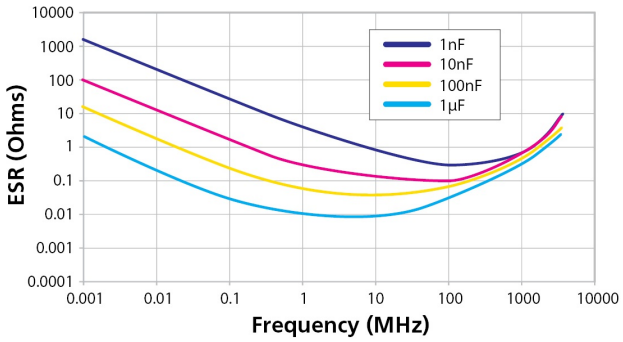



Typical TC Curves for X7R capacitors showing different dielectric types

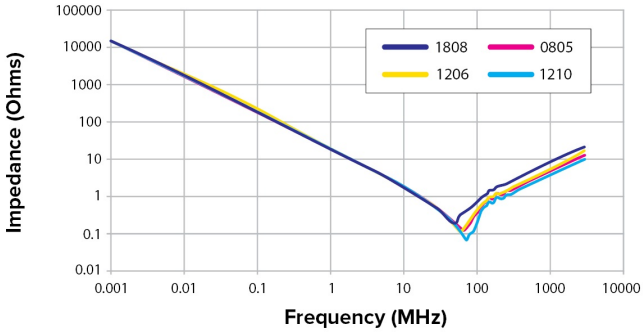
Stable X7R Dielectric




Stable X7R Dielectric




Stable X7R Dielectric — 10nF




Typical Performance Data - X7R

For part specific data, please contact your local sales office

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