Multilayer Ceramic Chip Capacitor

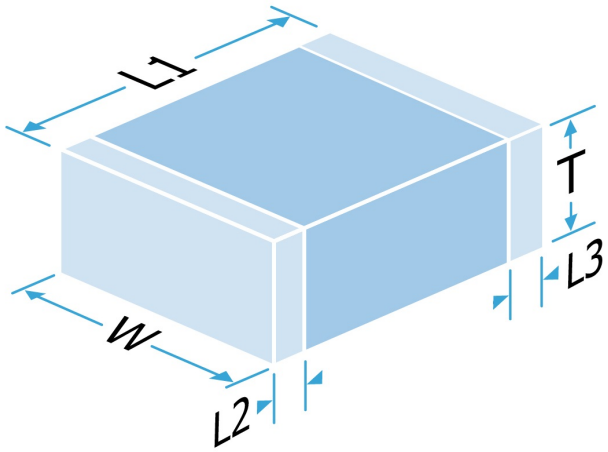
Part Number: 1812Y0250683FCT

Description: 1812 25Vdc 68nF ±1% C0G/NP0 (1B) (CTI ≥ 600)

A range of C0G/NP0 MLC capacitors to suit a variety of applications. Available in a wide selection of chip sizes, working voltages and termination options, including FlexiCap™, the world's first commercially available flexible termination.

Suffix code PXX or PX mandates the use of precious metal electrode (PME) materials. This may incur additional costs.

Parts suffix coded VM2 are designed and qualified for mounting as 1210 case size with increased thickness. Please refer to the factory to discuss mounting in alternative ways.



Mechanical Specification

Size Code	1812
Length (L1) in mm (")	4.5 +0.40/-0.30 (0.180 +0.016/-0.012)
Width (W) in mm (")	3.2 ± 0.20 (0.126 ± 0.008)
Thickness (T) in mm (")	2.5 Max (0.1 Max)
Minimum Termination Band (L2,L3) in mm (")	0.25 (0.010)
Maximum Termination Band (L2,L3) in mm (")	1.143 (0.045)
Termination Material	FlexiCap™ Polymer termination, Nickel barrier, Sn Plated Solder (RoHS compliant)
Solderability	IEC-60068-2-58
Packaging	7" Reel Horizontal Orientation, 500 per reel
Conformal Coating	Not normally required

General Electrical Specification

Rated Voltage	25Vdc
Nominal Capacitance Value	68nF
Capacitance Tolerance	±1%
Tangent of Loss Angle (Tan δ)	≤0.0015
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1kHz
Voltage Proof (Voltage applied for 5 secs max. @ 50mA max. charge current. 50% Max, RH)	63Vdc
Min Insulation Resistance (IR)	14.71GOhm @ 25Vdc
Dielectric Classification	C0G/NP0 (1B) (CTI ≥ 600)
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage 0±30ppm/°C Rated DC Voltage -
Climatic Category (IEC)	55/125/56
Ageing Characteristic	Zero

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This datasheet is for a standard item and is confirmed valid on the date generated, the latest published data for this part may differ and is available at http://www.knowlescapacitors.com or by contacting us.

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Data is correct to the best of our knowledge, errors and omissions excepted.

Date: Saturday, June 20, 2026

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Multilayer Ceramic Chip Capacitor

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Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU	Compliant
REACH Compliant	250 compliant
California Proposition 65	No exposure risk

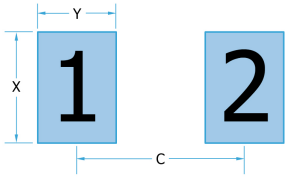
Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover, especially under high humidity conditions. Board cleanliness and environmental conditions can also impact this. Refer to application note AN0043 for further information.

IPC-7351 pad design

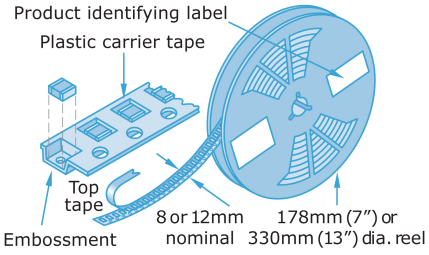
	1812	
C	4.00mm	0.157"
Y	1.55mm	0.061"
X	3.40mm	0.134"



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



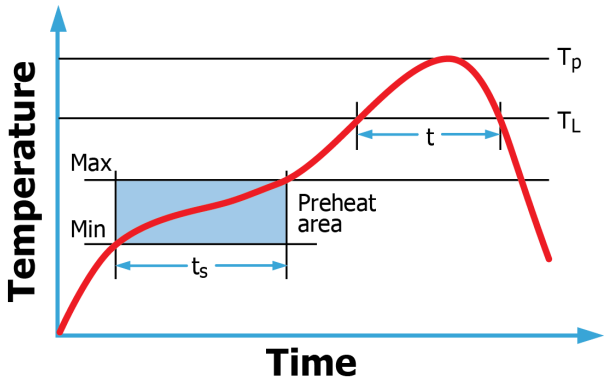
Soldering

Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.



Application notes with mounting and handling guidance are available on request.

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