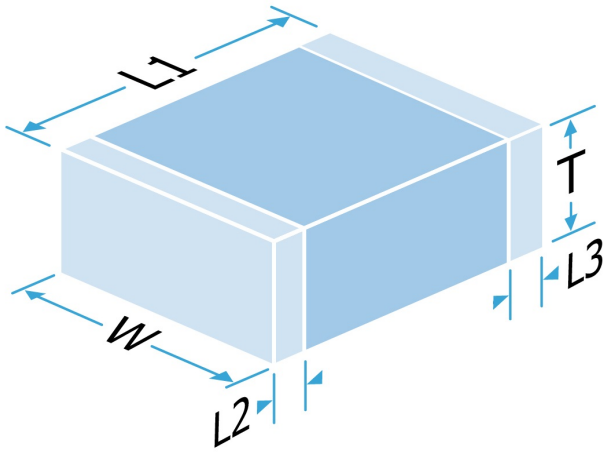
Multilayer Ceramic Chip Capacitor

Part Number: 1206J0500472JFT

Description: 1206 50Vdc 4.7nF ±5% C0G/NP0 (1B)

A range of MLC capacitors approved to IECQ-CECC QC32100 to support demanding applications such as aerospace or military. Available in 0603 to 2220 chip sizes with capacitance values up to 6.8uF as standard. A variety of termination options are available including FlexiCap™, the world's first commercially available flexible termination.



Mechanical Specification

Size Code	1206
Length (L1) in mm (")	3.2 ± 0.20 (0.126 ± 0.008)
Width (W) in mm (")	1.6 ± 0.20 (0.063 ± 0.008)
Thickness (T) in mm (")	1.6 Max (0.063 Max)
Minimum Termination Band (L2,L3) in mm (")	0.25 (0.010)
Maximum Termination Band (L2,L3) in mm (")	0.75 (0.030)
Termination Material	Nickel Barrier, Sn Plated Solder (RoHS compliant)
Solderability	IEC-60068-2-58
Packaging	7" Reel Horizontal Orientation, 2500 per reel

General Electrical Specification

Rated Voltage	50Vdc
Nominal Capacitance Value	4.7nF
Capacitance Tolerance	±5%
Tangent of Loss Angle (Tan δ)	≤0.0015
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1kHz
Voltage Proof (Voltage applied for 5 secs max. @ 50mA max. charge current. 50% Max, RH)	125Vdc
Min Insulation Resistance (IR)	100.00GOhm @ 50Vdc
Dielectric Classification	C0G/NP0 (1B)
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage 0±30ppm/°C Rated DC Voltage -
Climatic Category (IEC)	55/125/56
Ageing Characteristic	Zero

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This datasheet is for a standard item and is confirmed valid on the date generated, the latest published data for this part may differ and is available at http://www.knowlescapacitors.com or by contacting us.

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Data is correct to the best of our knowledge, errors and omissions excepted.

Date: Friday, June 19, 2026

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Multilayer Ceramic Chip Capacitor

Part Number: 1206J0500472JFT

Description: 1206 50Vdc 4.7nF ±5% C0G/NP0 (1B)

Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU	Compliant
REACH Compliant	250 compliant
California Proposition 65	No exposure risk

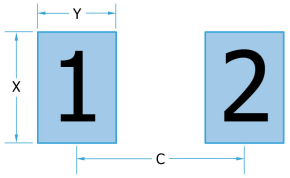
Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover, especially under high humidity conditions. Board cleanliness and environmental conditions can also impact this. Refer to application note AN0043 for further information.

IPC-7351 pad design

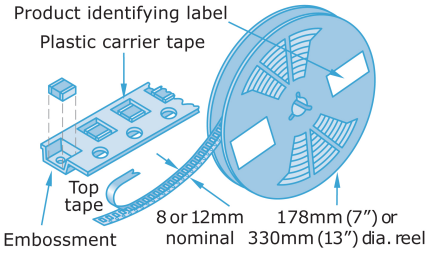
	1206	
C	3.00mm	0.118"
Y	1.15mm	0.045"
X	1.80mm	0.071"



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



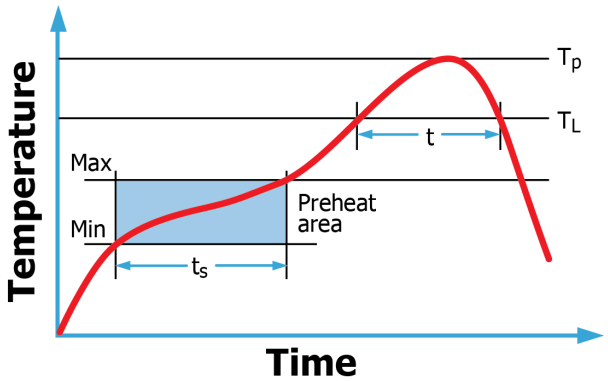
Soldering

Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.



Application notes with mounting and handling guidance are available on request.

Compex DLI Johanson MFG Novacap Syfer Voltronics

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