Overview

KEMET Power Solutions (KPS) Series stacked capacitors utilize a proprietary lead-frame technology to vertically stack one or two multilayer ceramic chip capacitors into a single compact surface mount package. The attached lead-frame mechanically isolates the capacitor's from the printed circuit board, therefore offering advanced mechanical and thermal stress performance. Isolation also addresses concerns for audible, microphonic noise that may occur when a bias voltage is applied. A two chip stack offers up to double the capacitance in the same or smaller design footprint when compared to traditional surface mount MLCC devices.

Combined with the stability of an X7R dielectric, KEMET's KPS Series devices exhibit a predictable change in capacitance with respect to time and voltage and boast a minimal change in capacitance with reference to ambient temperature. Capacitance change is limited to ±15% from -55°C to +125°C.

KPS Series automotive grade capacitors meet the demanding Automotive Electronics Council's AEC-Q200 qualification requirements.

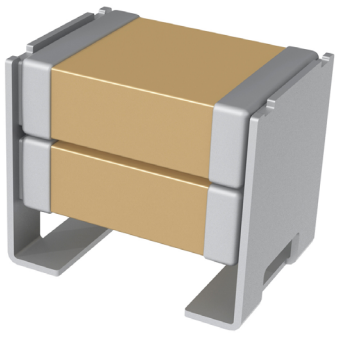
Benefits

- Commercial and Automotive Grade
- EIA 1210, 1812 & 2220 case sizes
- -55°C to +125°C operating temperature range
- DC voltage ratings of 10V, 16V, 25V, 50V, 100V, 250V, 500V, and 630V.
- Capacitance offerings ranging from 0.047µF up to 47µF
- Available capacitance tolerances of ±10% & ±20%
- Sn and SnPb Termination finish available[1]
- Higher capacitance in the same footprint
- Potential board space savings
- Advanced protection against thermal & mechanical stress
- Provides up to 10mm of board flex capability
- Reduces audible, microphonic noise
- Lead (Pb)-Free, RoHS and REACH compliant[2]
- Non-polar device, minimizing installation concerns
- Tantalum & electrolytic alternative

[1] SnPb finish only available in Commercial Grade
[2] With Sn termination finish.

Applications

- SMPS (Switch Mode Power Supplies)
- DC/DC Converters
- Telecom equipment
- Industrial and medical equipment
- Filtering
- Bypass



Ordering Information

C	2220	C	106	M	5	R	2	C	7186
Ceramic	Case Size (L" x W")	Specification/ Series	Capacitance Code (pF)	Capacitance Tolerance[1]	Rated Voltage (VDC)	Dielectric	Failure Rate/ Design	Leadframe Finish[2]	Packaging/ Grade (C-Spec)
	1210 1812 2220	C = Standard	2 Sig. Digits + Number of Zeros	K = ±10% M = ±20%	8 = 10 4 = 16 3 = 25 5 = 50 1 = 100 A = 250 C = 500 B = 630	R = X7R	1 = KPS Single Chip Stack 2 = KPS Double Chip Stack	C = 100% Matte Sn L = SnPb (5% Pb min.)	See "Packaging C-Spec Ordering Options Table"

[1] Double chip stacks ("2" in the 13th character position of the ordering code) are only available in M (±20%) capacitance tolerance. Single chip stacks ("1" in the 13th character position of the ordering code) are available in K (±10%) or M (±20%) tolerances.
[2] SnPb finish only available in Commercial Grade

Packaging C-Spec Ordering Options Table

Packaging Type[1]	Packaging/Grade Ordering Code (C-Spec)
Commercial Grade	
7" Reel (Embossed Plastic Tape)/Unmarked	7186
13" Reel (Embossed Plastic Tape)/Unmarked	7289
Automotive Grade	
7" Reel (Embossed Plastic Tape) / Unmarked	AUTO
13" Reel (Embossed Plastic Tape) / Unmarked	AUTO 7289

[1] The terms "Marked" and "Unmarked" pertain to laser marking option of capacitors. All packaging options labeled as "Unmarked" will contain capacitors that have not been laser marked. The option to laser mark is not available on these devices. For more information see "Capacitor Marking."
[2] For additional Information regarding "AUTO" C-Spec options, see "Automotive C-Spec Information".

Application Note

X7R dielectric is not recommended for AC line filtering or pulse applications.

Qualification/Certification

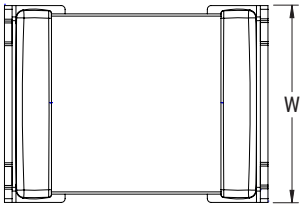
Commercial grade products are subject to internal qualification. Details regarding test methods and conditions are referenced in Table 4, Performance & Reliability.

Environmental Compliance

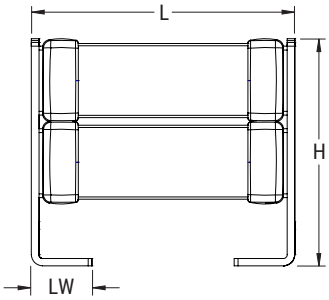
These devices do not meet RoHS criteria when orders with SnPb finish.

Dimensions – Inches (Millimeters)

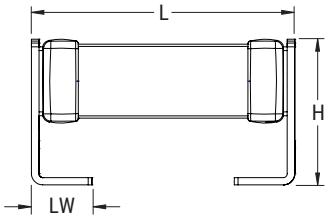
Single or Double Chip Stack



Double Chip Stack



Single Chip Stack



Number of Chips	EIA SIZE CODE	METRIC SIZE CODE	L LENGTH	W WIDTH	H HEIGHT	LW LEAD WIDTH	Mounting Technique
Single	1210	3225	3.50 (0.138) ±0.30 (0.012)	2.60 (0.102) ±0.30 (0.012)	3.35 (0.132) ±0.10 (0.004)	0.80 (0.032) ±0.15 (0.006)	Solder Reflow Only
	1812	4532	5.00 (0.197) ±0.50 (0.020)	3.50 (0.138) ±0.50 (0.020)	2.65 (0.104) ±0.35 (0.014)	1.10 (0.043) ±0.30 (0.012)	
	2220	5650	6.00 (0.236) ±0.50 (0.020)	5.00 (0.197) ±0.50 (0.020)	3.50 (0.138) ±0.30 (0.012)	1.60 (0.063) ±0.30 (0.012)	
Double	1210	3225	3.50 (0.138) ±0.30 (0.012)	2.60 (0.102) ±0.30 (0.012)	6.15 (0.242) ±0.15 (0.006)	0.80 (0.031) ±0.15 (0.006)	
	1812	4532	5.00 (0.197) ±0.50 (0.020)	3.50 (0.138) ±0.50 (0.020)	5.00 (0.197) ±0.50 (0.020)	1.10 (0.043) ±0.30 (0.012)	
	2220	5650	6.00 (0.236) ±0.50 (0.020)	5.00 (0.197) ±0.50 (0.020)	5.00 (0.197) ±0.50 (0.020)	1.60 (0.063) ±0.30 (0.012)	

Automotive C-Spec Information

KEMET Automotive Grade products meet or exceed the requirements outlined by the Automotive Electronics Council. Details regarding test methods and conditions are referenced in document AEC–Q200, Stress Test Qualification for Passive Components. These products are supported by a Product Change Notification (PCN) and Production Part Approval Process warrant (PPAP).

Automotive products offered through our distribution channel have been assigned an inclusive ordering code C-Spec, "9170." This C-Spec was developed in order to better serve small and medium sized companies that prefer an automotive grade component without the requirement to submit a customer Source Controlled Drawing (SCD) or specification for review by a KEMET engineering specialist. This C-Spec is therefore not intended for use by KEMET's OEM Automotive customers and are not granted the same "privileges" as other automotive C-Specs. Customer PCN approval and PPAP request levels are limited (see details below).

Product Change Notification (PCN)

The KEMET Product Change Notification system is used to communicate primarily the following types of changes:

- Product/process changes that affect product form, fit, function, and/or reliability
- Changes in manufacturing site
- Product obsolescence

KEMET Automotive C-Spec	Customer Notification due to:		Days prior to implementation
	Process/Product change	Obsolescence*	
KEMET assigned[1]	Yes (with approval and sign off)	Yes	180 days Minimum
AUTO	Yes (without approval)	Yes	90 days Minimum

[1] KEMET assigned C-Specs require the submittal of a customer SCD or customer specification for review. For additional information contact KEMET.

Production Part Approval Process (PPAP)

The purpose of the Production Part Approval Process is:

- To ensure that supplier can meet the manufacturability and quality requirements for the purchased parts.
- To provide the evidence that all customer engineering design record and specification requirements are properly understood and fulfilled by the manufacturing organization.
- To demonstrate that the established manufacturing process has the potential to produce the part

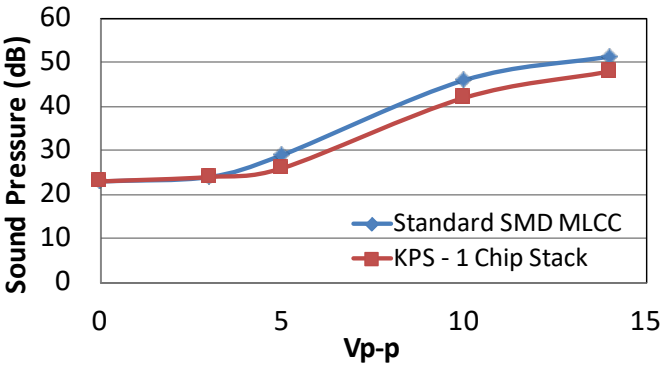
KEMET Automotive C-Spec	PPAP Level				
	1	2	3	4	5
KEMET assigned[1]	●	●	●	●	●
AUTO			○		

[1] KEMET assigned C-Specs require the submittal of a customer SCD or customer specification for review. For additional information contact KEMET.

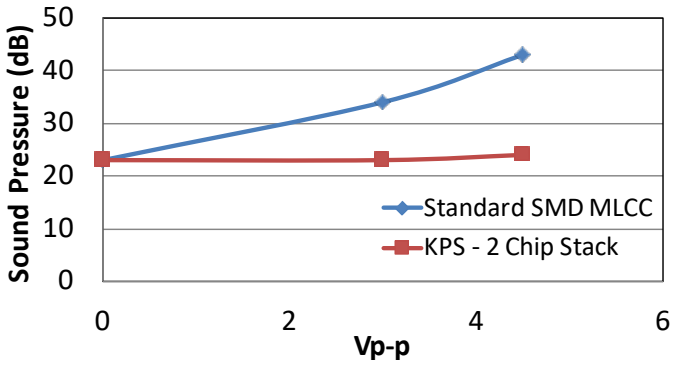
● Part number specific PPAP available with customer information included.
○ Product family PPAP only

Electrical Characteristics

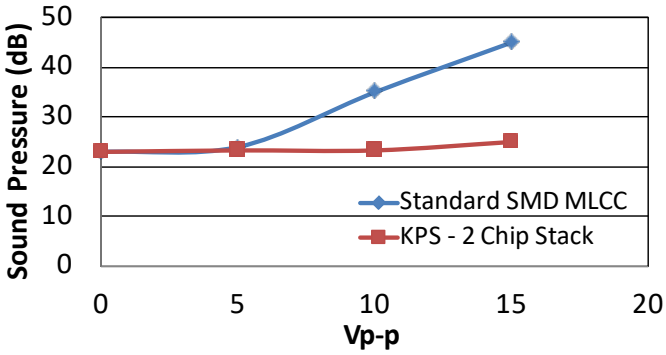
Microphonics – 1210, 4.7 µF, 50 V, X7R



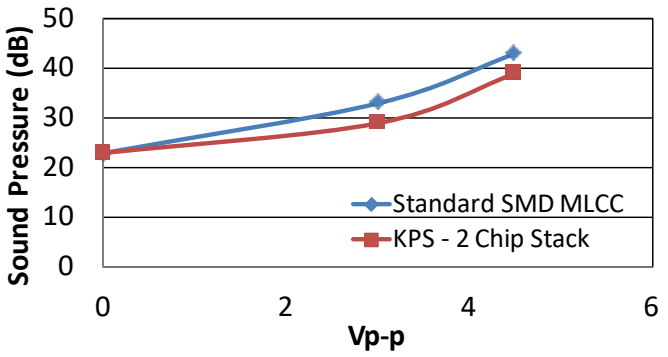
Microphonics – 2220, 22 µF, 50 V, X7R



Microphonics – 2220, 47 µF, 25 V, X7R

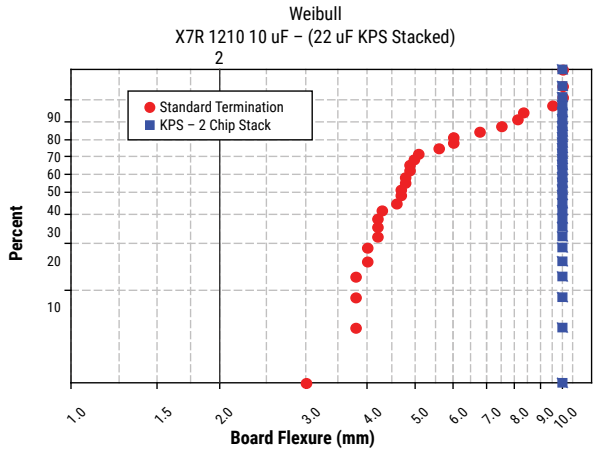


Microphonics – 1210, 22 µF, 25 V, X7R

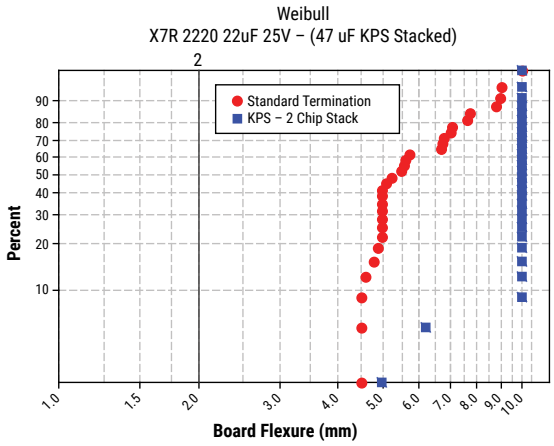


Electrical Characteristics cont.

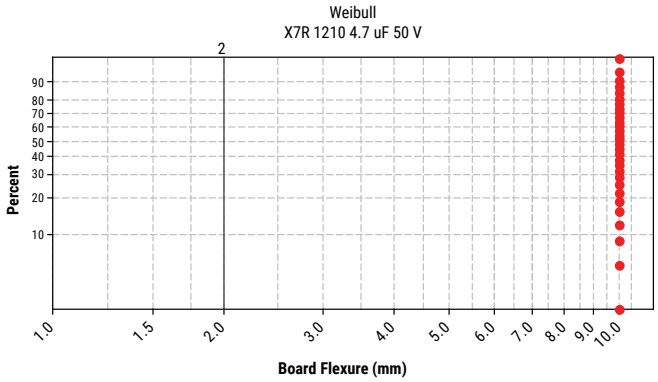
Board Flex vs. Termination Type



Board Flex vs. Termination Type



Board Flexure to 10 mm



Board Flexure to 10 mm

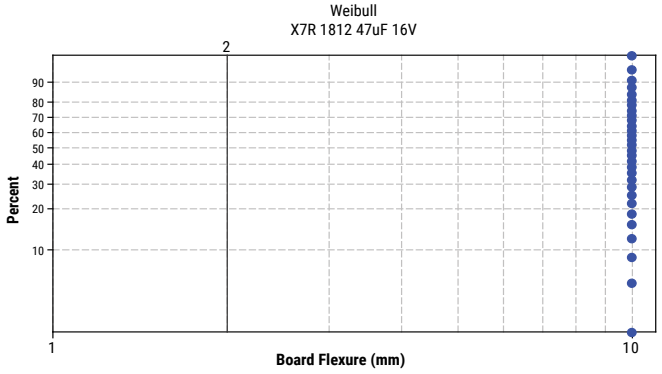


Table 1A – Capacitance Range/Selection Waterfall (Commercial Grade / Sn Termination)

Capacitance	Cap Code	Case Size/ Series		C1210C						C1812C					C2220C						
		Voltage Code		8	4	3	5	1	A	4	3	5	1	A	4	3	5	1	A	C	B
		Rated Voltage (VDC)		10	16	25	50	100	250	16	25	50	100	250	16	25	50	100	250	500	630
		Capacitance Tolerance		Product Availability and Chip Thickness Codes – See Table 2 for Chip Thickness Dimensions																	
Single Chip Stack																					
0.047 uF	473	K	M																	JP	JP
0.1 uF	104	K	M	FV	FV	FV	FV	FV	FV	GP	GP	GP	GP	GP	JP	JP	JP	JP	JP	JP	JP
0.15 uF	154	K	M																	JP	JP
0.22 uF	224	K	M	FV	FV	FV	FV	FV		GP	GP	GP	GP	GP	JP	JP	JP	JP	JP	JP	JP
0.33 uF	334	K	M																	JP	
0.47 uF	474	K	M	FV	FV	FV	FV	FV		GP	GP	GP	GP	GP	JP	JP	JP	JP	JP	JP	
1.0 uF	105	K	M	FV	FV	FV	FV	FV		GP	GP	GP	GP		JP	JP	JP	JP	JP		
2.2 uF	225	K	M	FV	FV	FV	FV	FV		GP	GP	GP			JP	JP	JP	JP			
3.3 uF	335	K	M	FV	FV	FV	FV			GP	GP	GP			JP	JP	JP	JP			
4.7 uF	475	K	M	FV	FV	FV	FV			GP	GP	GP			JP	JP	JP				
10 uF	106	K	M	FV	FV	FV				GP	GP				JP	JP	JP				
15 uF	156	K	M	FV											JP	JP					
22 uF	226	K	M	FV											JP	JP					
Double Chip Stack																					
0.1 Uf	104		M	FW	FW	FW	FW	FW	FW	GR	GR	GR	GR	GR	JR	JR	JR	JR	JR	JR	JR
0.22 uF	224		M	FW	FW	FW	FW	FW	FW	GR	GR	GR	GR	GR	JR	JR	JR	JR	JR	JR	JR
0.33 uF	334		M																	JR	JR
0.47 uF	474		M	FW	FW	FW	FW	FW		GR	GR	GR	GR	GR	JR	JR	JR	JR	JR	JR	JR
0.68 uF	684		M																	JR	
1.0 uF	105		M	FW	FW	FW	FW	FW		GR	GR	GR	GR	GR	JR	JR	JR	JR	JR	JR	
2.2 uF	225		M	FW	FW	FW	FW	FW		GR	GR	GR	GR		JR	JR	JR	JR	JR		
3.3 uF	335		M	FW	FW	FW	FW	FW		GR	GR	GR	GR		JR	JR	JR	JR			
4.7 uF	475		M	FW	FW	FW	FW	FW		GR	GR	GR			JR	JR	JR	JR			
10 uF	106		M	FW	FW	FW	FW			GR	GR	GR			JR	JR	JR				
22 uF	226		M	FW	FW	FW				GR	GR				JR	JR	JR				
33 uF	336		M	FW											JR	JR					
47 uF	476		M	FW											JR	JR					
Capacitance	Cap Code	Rated Voltage (VDC)		10	16	25	50	100	250	16	25	50	100	250	16	25	50	100	250	500	630
		Voltage Code		8	4	3	5	1	A	4	3	5	1	A	4	3	5	1	A	C	B
		Case Size/ Series		C1210C						C1812C					C2220C						

Table 1B – Capacitance Range/Selection Waterfall (Commercial Grade / SnPb Termination)

Capacitance	Capacitance Code	Case Size/ Series		C1210C						C2220C							
		Voltage Code		8	4	3	5	1	A	4	3	5	M	1	A	C	B
		Rated Voltage (VDC)		10	16	25	50	100	250	16	25	50	63	100	250	500	630
		Capacitance Tolerance		Product Availability and Chip Thickness Codes See Table 2 for Chip Thickness Dimensions													
Single Chip Stack																	
0.047 uF	473	K	M													JP	JP
0.1 uF	104	K	M	FV	FV	FV	FV	FV	FV	JP	JP	JP	JP	JP	JP	JP	JP
0.15 uF	154	K	M													JP	JP
0.22 uF	224	K	M	FV	FV	FV	FV	FV		JP	JP	JP	JP	JP	JP	JP	JP
0.33 uF	334	K	M													JP	
0.47 uF	474	K	M	FV	FV	FV	FV	FV		JP	JP	JP	JP	JP	JP	JP	
1.0 uF	105	K	M	FV	FV	FV	FV	FV		JP	JP	JP	JP	JP	JP		
2.2 uF	225	K	M	FV	FV	FV	FV			JP	JP	JP	JP	JP			
3.3 uF	335	K	M	FV	FV	FV	FV			JP	JP	JP	JP	JP			
4.7 uF	475	K	M	FV	FV	FV	FV			JP	JP	JP	JP				
10 uF	106	K	M	FV	FV	FV				JP	JP	JP	JP				
15 uF	156	K	M	FV						JP	JP						
22 uF	226	K	M	FV						JP	JP						
Double Chip Stack																	
0.1 uF	104		M	FW	FW	FW	FW	FW	FW	JR	JR	JR	JR	JR	JR	JR	JR
0.22 uF	224		M	FW	FW	FW	FW	FW	FW	JR	JR	JR	JR	JR	JR	JR	JR
0.33 uF	334		M													JR	JR
0.47 uF	474		M	FW	FW	FW	FW	FW		JR	JR	JR	JR	JR	JR	JR	JR
0.68 uF	684		M													JR	
1.0 uF	105		M	FW	FW	FW	FW	FW		JR	JR	JR	JR	JR	JR	JR	
2.2 uF	225		M	FW	FW	FW	FW	FW		JR	JR	JR	JR	JR	JR		
3.3 uF	335		M	FW	FW	FW	FW	FW		JR	JR	JR	JR	JR			
4.7 uF	475		M	FW	FW	FW	FW			JR	JR	JR	JR	JR			
10 uF	106		M	FW	FW	FW	FW			JR	JR	JR	JR				
22 uF	226		M	FW	FW	FW				JR	JR	JR	JR				
33 uF	336		M	FW						JR	JR						
47 uF	476		M	FW						JR	JR						
47 µF	476		M	FW						JR	JR						
Capacitance	Capacitance Code	Rated Voltage (VDC)		10	16	25	50	100	250	16	25	50	63	100	250	500	630
		Voltage Code		8	4	3	5	1	A	4	3	5	M	1	A	C	B
		Case Size/ Series		C1210C						C2220C							

Table 1C – Capacitance Range/Selection Waterfall (Automotive Grade)

Capacitance	Cap Code	Case Size/ Series		C1210C						C1812C					C2220C						
		Voltage Code		8	4	3	5	1	A	4	3	5	1	A	4	3	5	1	A	C	B
		Rated Voltage (VDC)		10	16	25	50	100	250	16	25	50	100	250	16	25	50	100	250	500	630
		Capacitance Tolerance		Product Availability and Chip Thickness Codes – See Table 2 for Chip Thickness Dimensions																	
Single Chip Stack																					
0.047 uF	473	K	M																	JP	JP
0.1 uF	104	K	M	FV	FV	FV	FV	FV	FV	GP	GP	GP			JP	JP	JP	JP	JP	JP	JP
0.15 uF	154	K	M																	JP	JP
0.22 uF	224	K	M	FV	FV	FV	FV	FV		GP	GP	GP			JP	JP	JP	JP	JP	JP	JP
0.33 uF	334	K	M																		
0.47 uF	474	K	M	FV	FV	FV	FV	FV		GP	GP	GP			JP	JP	JP				
1.0 uF	105	K	M	FV	FV	FV	FV	FV		GP	GP	GP			JP	JP	JP				
2.2 uF	225	K	M	FV	FV	FV	FV			GP	GP	GP			JP	JP	JP				
3.3 uF	335	K	M	FV	FV	FV	FV			GP	GP	GP			JP	JP	JP				
4.7 uF	475	K	M	FV	FV	FV	FV			GP	GP	GP			JP	JP	JP				
10 uF	106	K	M	FV	FV	FV				GP	GP				JP	JP	JP				
15 uF	156	K	M												JP	JP					
22 uF	226	K	M												JP	JP					
Double Chip Stack																					
0.1 uF	104		M	FW	FW	FW	FW	FW	FW	GR	GR	GR			JR	JR	JR	JR	JR	JR	JR
0.22 uF	224		M	FW	FW	FW	FW	FW	FW	GR	GR	GR			JR	JR	JR	JR	JR	JR	JR
0.33 uF	334		M																	JR	JR
0.47 uF	474		M	FW	FW	FW	FW	FW		GR	GR	GR			JR	JR	JR	JR	JR	JR	JR
0.68 uF	684		M																		
1.0 uF	105		M	FW	FW	FW	FW	FW		GR	GR	GR			JR	JR	JR				
2.2 uF	225		M	FW	FW	FW	FW	FW		GR	GR	GR			JR	JR	JR				
3.3 uF	335		M	FW	FW	FW	FW			GR	GR	GR			JR	JR	JR				
4.7 uF	475		M	FW	FW	FW	FW			GR	GR	GR			JR	JR	JR				
10 uF	106		M	FW	FW	FW	FW			GR	GR	GR			JR	JR	JR				
22 uF	226		M	FW	FW	FW				GR	GR				JR	JR	JR				
33 uF	336		M												JR	JR					
47 uF	476		M												JR	JR					
Capacitance	Cap Code	Rated Voltage (VDC)		10	16	25	50	100	250	16	25	50	100	250	16	25	50	100	250	500	630
		Voltage Code		8	4	3	5	1	A	4	3	5	1	A	4	3	5	1	A	C	B
		Case Size/ Series		C1210C						C1812C					C2220C						

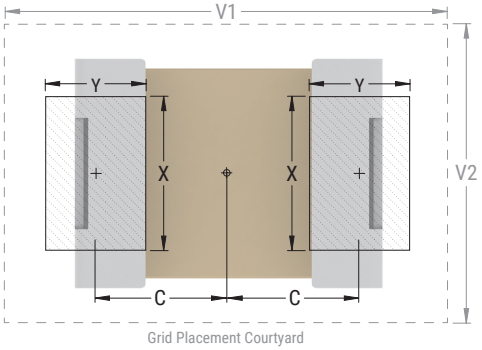
Table 2 – Chip Thickness/Tape & Reel Packaging Quantities

Thickness Code	Case Size	Thickness ± Range (mm)	Reel Quantity	
			7" Reel	13" Reel
FV	1210	3.35 ± 0.10	600	2,000
FW	1210	6.15 ± 0.15	300	1,000
GP	1812	2.65 ± 0.35	500	2,000
GR	1812	5.00 ± 0.50	400	1,700
JP	2220	3.50 ± 0.30	300	1,300
JR	2220	5.00 ± 0.50	200	800
Thickness Code	Case Size	Thickness ± Range (mm)	7" Reel	13" Reel
			Reel Quantity	

Package quantity based on finished chip thickness specifications.

Table 3 – KPS Land Pattern Design Recommendations (mm)

EIA SIZE CODE	METRIC SIZE CODE	Median (Nominal) Land Protrusion				
		C	Y	X	V1	V2
1210	3225	1.50	1.14	1.75	5.05	3.40
1812	4532	2.20	1.35	2.87	6.70	4.50
2220	5650	2.69	2.08	4.78	7.70	6.00



KEMET's KPS Series land pattern design recommendations have been evaluated through extensive internal testing and validation. KPS lead frames are used to mechanically isolate the MLCC from the PCB and provide stress relief for increased mechanical robustness. The land pattern dimensions for each EIA size code are designed to be encompassed within the end terminations thus regulating solder wicking and maintaining lead frame flexibility. This design is optimized to enable durable solder joint fillets which improve the mechanical integrity and reliability upon placement.

Soldering Process

KEMET's KPS devices are compatible with IR reflow techniques. Preheating of these components is recommended to avoid extreme thermal stress. KEMET's recommended profile conditions for IR reflow reflect the profile conditions of the IPC/J-STD-020D standard for moisture sensitivety testing.

To prevent degradation of temperature cycling capability, care must be taken to prevent solder from flowing into the inner side of the lead frames (inner side of "J" lead in contact with the circuit board).

After soldering, the capacitors should be air cooled to room temperature before further processing. Forced air cooling is not recommended.

Hand soldering should be performed with care due to the difficulty in process control. If performed, care should be taken to avoid contact of the soldering iron to the capacitor body. The iron should be used to heat the solder pad, applying solder between the pad and the lead, until reflow occurs. Once reflow occurs, the iron should be removed immediately. (Preheating is required when hand soldering to avoid thermal shock.)

Profile Feature	SnPb Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Minimum (T_{Smin})	100°C	150°C
Temperature Maximum (T_{Smax})	150°C	200°C
Time (t_s) from T_{smin} to T_{smax})	60 – 120 seconds	60 – 120 seconds
Ramp-up Rate (T_L to T_P)	3°C/seconds maximum	3°C/seconds maximum
Liquidous Temperature (T_L)	183°C	217°C
Time Above Liquidous (t_L)	60 – 150 seconds	60 – 150 seconds
Peak Temperature (T_P)	235°C	250°C
Time within 5°C of Maximum Peak Temperature (t_P)	20 seconds maximum	10 seconds maximum
Ramp-down Rate (T_P to T_L)	6°C/seconds maximum	6°C/seconds maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

Note: All temperatures refer to the center of the package, measured on the capacitor body surface that is facing up during assembly reflow.

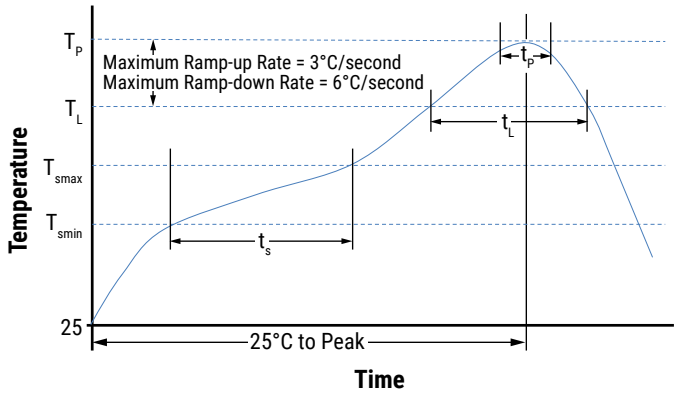


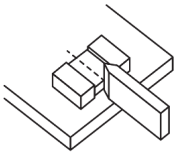
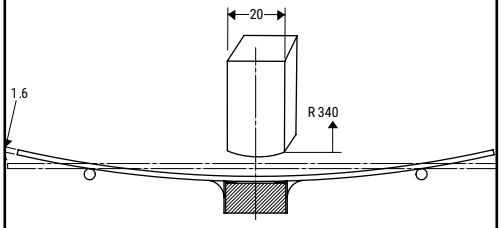
Table 4 – Performance & Reliability: Test Methods & Conditions

<table>
<tr><th>TEST</th><th>REFERENCE</th><th>TEST CONDITIONS</th><th>LIMITS</th></tr>
<tr><td>Visual & Mechanical</td><td>KEMET Internal</td><td>No defects that may affect performance (10X)</td><td>Dimensions according KEMET Spec Sheet</td></tr>
<tr><td>Capacitance (Cap)</td><td>KEMET Internal</td><td>1 kHz ±50 Hz and 1.0 ±0.2 Vrms if capacitance ≤ 10 µF
120 Hz ±10 Hz and 0.5 ±0.1 Vrms if capacitance > 10 µF</td><td>Within Tolerance

Note: When measuring capacitance it is important to ensure the set voltage level is held constant. The HP4284 & Agilent E4980 have a feature known as Automatic Level Control (ALC). The ALC feature should be switched to "ON".</td></tr>
<tr><td>Dissipation Factor (DF)</td><td>KEMET Internal</td><td>1 kHz ±50 Hz and 1.0 ±0.2 Vrms if capacitance ≤ 10 µF
120 Hz ±10 Hz and 0.5 ±0.1 Vrms if capacitance > 10 µF</td><td>Within Specification
<table><tr><th colspan="2">DF Limits Maximum (%)</th></tr><tr><th>Voltage</th><th>Initial</th></tr><tr><td>> 25</td><td>2.5</td></tr><tr><td>16/25</td><td>3.5</td></tr><tr><td>< 16</td><td>5</td></tr></table></td></tr>
<tr><td>Insulation Resistance (IR)</td><td>KEMET Internal</td><td>Apply rated voltage for 120 seconds at 25oC</td><td>Within Specification
To obtain IR limit, divide MΩ-µF value by the capacitance and compare to GΩ limit. Select the lower of the two limits.
<table><tr><th>EIA Case Size</th><th>Stack</th><th>Voltage</th><th>1,000 Megohm Microfarads or 100 G</th><th>500 Medohm Microfarads or 10G</th><th>100 Megohm Microfarads or 1G</th></tr><tr><td>1210</td><td>Single / Double</td><td>16 - 250</td><td>< 0.39 µF</td><td>≥ 0.39 µF</td><td></td></tr><tr><td>1812</td><td>Single / Double</td><td>16-250</td><td>< 2.2 µF</td><td>≥ 2.2 µF</td><td></td></tr><tr><td>2220</td><td>Single / Double</td><td>16-250</td><td>< 10 µF</td><td>≥ 10 µF</td><td></td></tr><tr><td>2220</td><td>Single</td><td>≥ 500</td><td>≤ 0.22 µF</td><td></td><td>≥ 0.33 µF</td></tr><tr><td>2220</td><td>Double</td><td>≥ 500</td><td>≤ 0.47 µF</td><td></td><td>≥ 0.68 µF</td></tr></table></td></tr>
<tr><td>Temperature Coefficient of Capacitance (TCC)</td><td>KEMET Internal</td><td>1 kHz ±50 Hz and 1.0 ±0.2 Vrms if capacitance ≤ 10 µF
120 Hz ±10 Hz and 0.5 ±0.1 Vrms if capacitance > 10 µF
<table><tr><th>Step</th><th>Temperature (°C)</th></tr><tr><td>1</td><td>+25°C</td></tr><tr><td>2</td><td>−55°C</td></tr><tr><td>3</td><td>+25°C (Reference Temperature)</td></tr><tr><td>4</td><td>+125°C</td></tr></table></td><td>Capacitance ±15% over −55°C to +125°C</td></tr>
<tr><td>Dielectric Withstanding Voltage (DWV)</td><td>KEMET Internal</td><td>250% of rated voltage for voltage rating ≤250V
150% of rated voltage for voltage rating 500V and 630V

(5 ±1 seconds and charge/discharge not exceeding 50 mA)</td><td>Withstand test voltage without insulation breakdown or damage.</td></tr>
<tr><td>Aging Rate (Maximum % Capacitance Loss/ Decade Hour)</td><td>KEMET Internal</td><td>3.0% Capacitance Loss / Decade Hour
Capacitance measurements (including tolerance) are indexed to a referee time of 1,000 hours.</td><td>Please refer to a part number specification sheet for specific Aging rate</td></tr>
</table>

Table 4 – Performance & Reliability: Test Methods & Conditions cont.

<table>
<tr><td>Terminal Strength</td><td>KEMET Internal</td><td>Shear stress test per specific case size, Time: 60±1 sec.
Force: 18N
</td><td>No evidence of mechanical damage</td></tr>
<tr><td>Board Flex</td><td>AEC-Q200-005</td><td>5.0mm Minimum
Test time: 60± 5sec Ramp time: 1 mm / sec

</td><td>No evidence of mechanical damage</td></tr>
<tr><td>Solderability</td><td>J-STD-002</td><td>Condition: 4 hours ± 15 minutes at 155°C dry bake apply all methods
Test 245 ±5°C (SnPb & Pb-Free)</td><td>Visual Inspection. 95% coverage on termination. No leaching</td></tr>
<tr><td>Temperature Cycling</td><td>JESD22 Method JA-104</td><td>1,000 cycles (-55°C to +125°C)
2-3 cycles per hour
Soak Time 1 or 5 min</td><td>Measurement at 24 hours ±4 hours after test conclusion.
Cap: ±20% shift
DF: Initial Limit
IR: Initial Limit</td></tr>
<tr><td>Biased Humidity</td><td>MIL-STD-202 Method 103</td><td>Load Humidity:
1,000 hours 85°C / 85% RH and rated voltage.

Low Volt Humidity:
1,000 hours 85°C / 85% RH and 1.5 V.</td><td>Measurement at 24 hours ±4 hours after test conclusion.
Within Post Environmental Limits
Cap: ±20% shift
IR: 10% of Initial Limit

DF Limits Maximum (%)
<table><tr><th>Voltage</th><th>Initial</th><th>Initial</th></tr><tr><td>> 25</td><td>2.5</td><td>3.0</td></tr><tr><td>16/25</td><td>3.5</td><td>5.0</td></tr><tr><td>< 16</td><td>5</td><td>7.5</td></tr></table></td></tr>
<tr><td>Thermal Shock</td><td>MIL-STD-202 Method 107</td><td>Number of cycles required 5, (-55°C to 125°C)
Dwell time 15 minutes.</td><td>Cap:±20% shift
DF: Initial Limit
IR: Initial Limit</td></tr>
</table>

Table 4 – Performance & Reliability: Test Methods & Conditions cont.

<table>
<tr><td>High Temperature Life</td><td>MIL-STD-202 Method 108</td><td>150% of rated voltage for voltage rating ≤250V
100% of rated voltage for voltage rating ≥500V

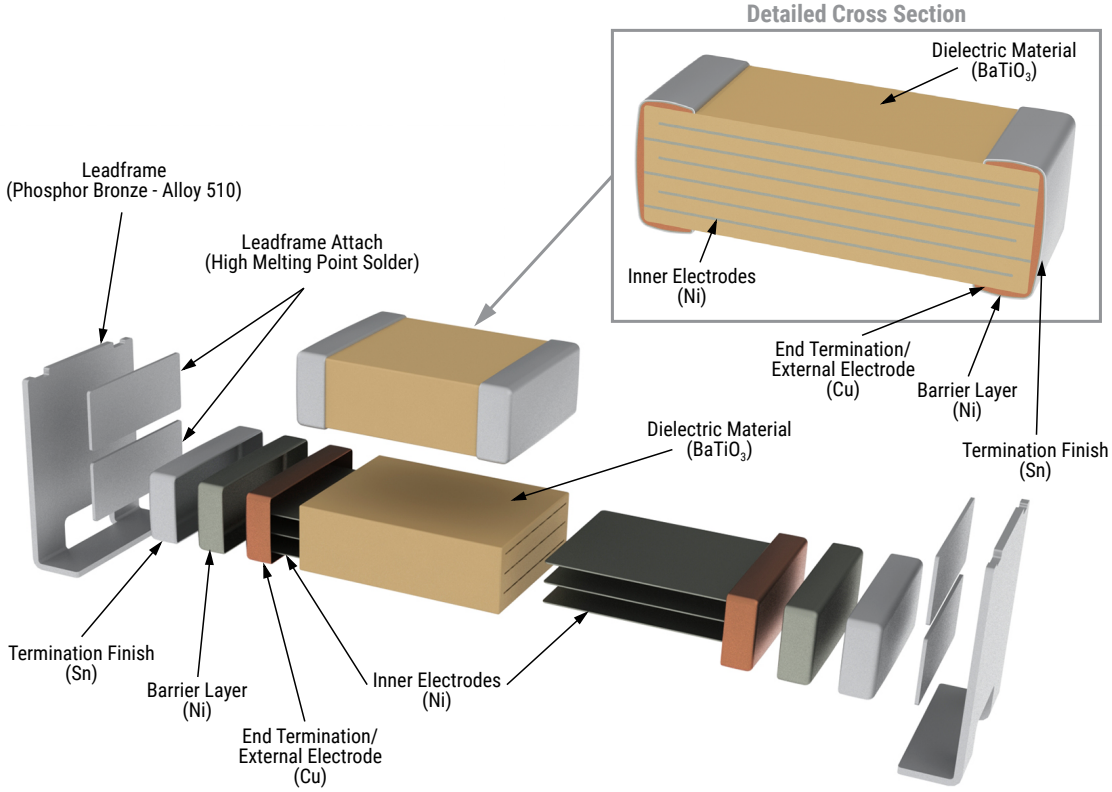
1,000 hours at 125°C</td><td>Within Post Environmental Limits
Cap: ±20% shift
IR: 10% of Initial Limit
<table><tr><th colspan="3">DF Limits Maximum (%)</th></tr><tr><th>Voltage</th><th>Initial</th><th>Initial</th></tr><tr><td>> 25</td><td>2.5</td><td>3.0</td></tr><tr><td>16/25</td><td>3.5</td><td>5.0</td></tr><tr><td>< 16</td><td>5</td><td>7.5</td></tr></table></td></tr>
<tr><td>Vibration</td><td>MIL-STD-202 Method 204</td><td>5 g's for 20 minutes, 12 cycles each of 3 orientations. Test from 10 – 2,000 Hz</td><td>Cap: ±20% shift
DF: Initial Limit
IR: Initial Limit</td></tr>
<tr><td>Resistance to Soldering Heat</td><td>MIL-STD-202 Method 210</td><td>Condition K, time above 217°C, 60s – 150s</td><td>Cap: ±20% shift
DF: Initial Limit
IR: Initial Limit</td></tr>
</table>

Storage & Handling

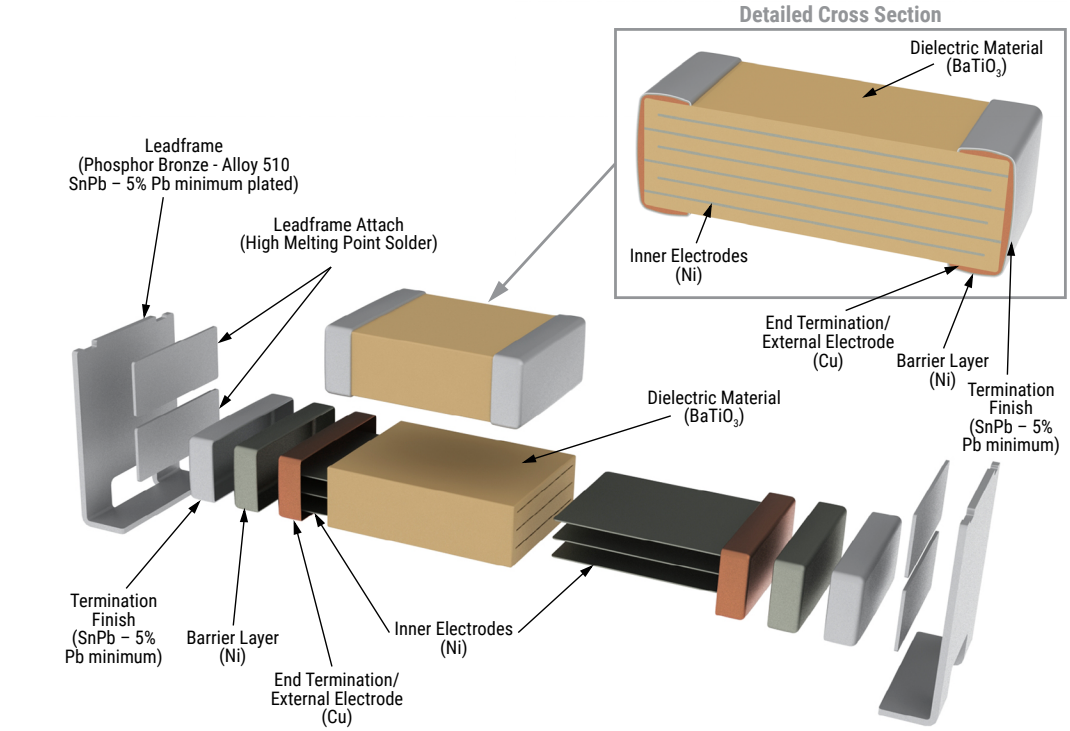
Ceramic chip capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature – reels may soften or warp and tape peel force may increase. KEMET recommends that maximum storage temperature not exceed 40°C and maximum storage humidity not exceed 70% relative humidity. In addition, temperature fluctuations should be minimized to avoid condensation on the parts and atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability chip stock should be used promptly, preferably within 1.5 years of receipt.

Construction

Construction - Sn Termination Finish



Construction - SnPbs Termination Finish



Tape & Reel Packaging Information

KEMET offers multilayer ceramic chip capacitors packaged in 8, 12 and 16 mm tape on 7" and 13" reels in accordance with EIA Standard 481. This packaging system is compatible with all tape-fed automatic pick and place systems. See Table 2 for details on reeling quantities for commercial chips.

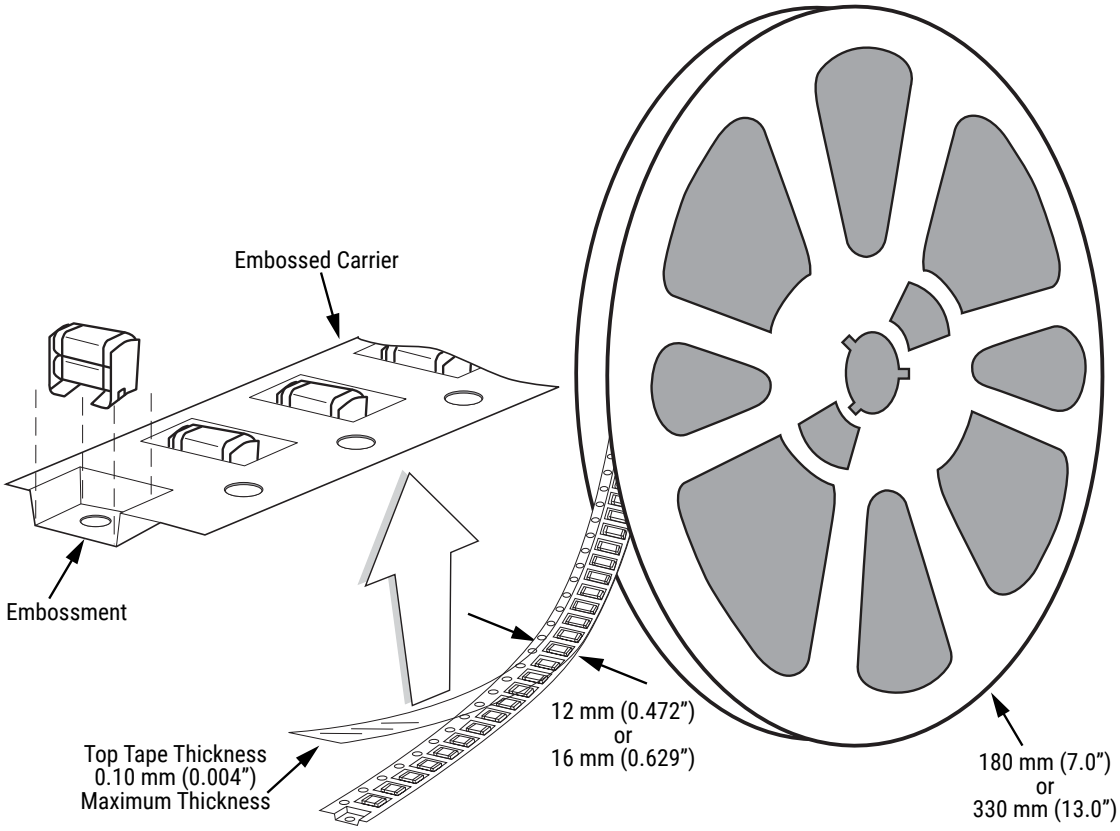


Table 5 – Carrier Tape Configuration – Embossed Plastic (mm)

EIA Case Size	Tape Size (W)*	Pitch (P_1)*	
KPS 1210	12	8	8
KPS 1812 & 2220	16	12	12

**Refer to Figure 1 for W and P_1 carrier tape reference locations.*
**Refer to Table 5 for tolerance specifications.*

Figure 1 – Embossed (Plastic) Carrier Tape Dimensions

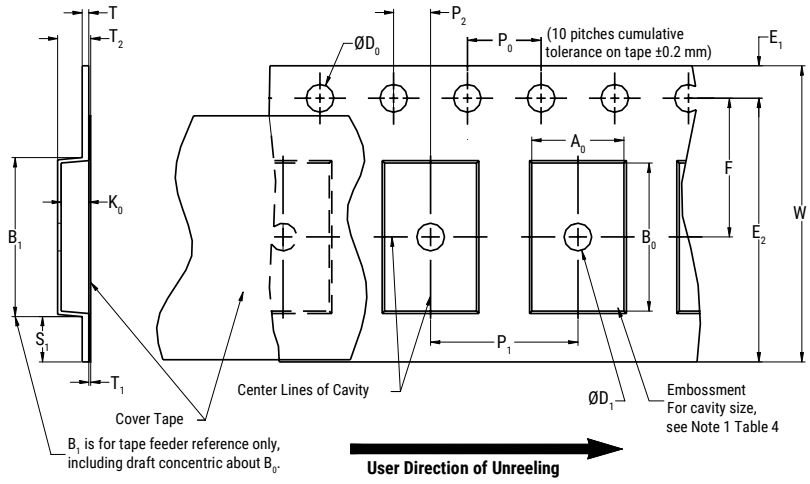


Table 6 – Embossed (Plastic) Carrier Tape Dimensions

Metric will govern

Constant Dimensions — Millimeters (Inches)									
Tape Size	D_0	D_1 Minimum Note 1	E_1	P_0	P_2	R Reference Note 2	S_1 Minimum Note 3	T Maximum	T_1 Maximim
8 mm	1.5 +0.10/0.0–0.0 (0.059 +0.004/–0.0)	1.0 (0.039)	1.75 ±0.10 (0.069 ±0.004)	4.0 ±0.10 (0.157 ±0.004)	2.0 ±0.05 (0.079 ±0.002)	25.0 (0.984)	0.600 (0.024)	0.600 (0.024)	0.100 (0.004)
12 mm		1.5 (0.059)				30 (1.181)			
16 mm									

Variable Dimensions — Millimeters (Inches)								
Tape Size	Pitch	B_1 Maximum Note 4	E_2 Minimum	F	P_1	T_2 Maximum	W Maximum	A_0, B_0 & K_0
8 mm	Single (4 mm)	4.35 (0.171)	6.25 (0.246)	3.5 ±0.05 (0.138 ±0.002)	4.0 ±0.10 (0.157 ±0.004)	2.5 (0.098)	8.3 (0.327)	Note 5
12 mm	Single (4 mm) and Double (8 mm)	8.2 (0.323)	10.25 (0.404)	5.5 ±0.05 (0.217 ±0.002)	8.0 ±0.10 (0.315 ±0.004)	4.6 (0.181)	12.3 (0.484)	
16 mm	Triple (12 mm)	12.1 (0.476)	14.25 (0.561)	7.5 ±0.05 (0.138 ±0.002)	12.0 ±0.10 (0.157 ±0.004)	4.6 (0.181)	16.3 (0.642)	

1. The embossment hole location shall be measured from the sprocket hole controlling the location of the embossment. Dimensions of embossment location and hole location shall be applied independent of each other.

2. The tape with or without components shall pass around R without damage (see Figure 5).

3. If S_1 < 1.0 mm, there may not be enough area for cover tape to be properly applied (see EIA Standard 481 paragraph 4.3 section b).

4. B_1 dimension is a reference dimension for tape feeder clearance only.

5. The cavity defined by A_0, B_0 and K_0 shall surround the component with sufficient clearance that:

(a) the component does not protrude above the top surface of the carrier tape.

(b) the component can be removed from the cavity in a vertical direction without mechanical restriction, after the top cover tape has been removed.

(c) rotation of the component is limited to 20° maximum for 8 and 12 mm tapes and 10° maximum for 16 mm tapes (see Figure 2).

(d) lateral movement of the component is restricted to 0.5 mm maximum for 8 and 12 mm wide tape and to 1.0 mm maximum for 16 mm tape (see Figure 3).

(e) for KPS Series product, A_0 and B_0 are measured on a plane 0.3 mm above the bottom of the pocket.

(f) see Addendum in EIA Standard 481 for standards relating to more precise taping requirements.

Packaging Information Performance Notes

1. Cover Tape Break Force: 1.0 kg minimum.
2. Cover Tape Peel Strength: The total peel strength of the cover tape from the carrier tape shall be:

Tape Width	Peel Strength
8 mm	0.1 to 1.0 newton (10 to 100 gf)
12 and 16 mm	0.1 to 1.3 newton (10 to 130 gf)

The direction of the pull shall be opposite the direction of the carrier tape travel. The pull angle of the carrier tape shall be 165° to 180° from the plane of the carrier tape. During peeling, the carrier and/or cover tape shall be pulled at a velocity of 300 ±10 mm/minute.
3. Labeling: Bar code labeling (standard or custom) shall be on the side of the reel opposite the sprocket holes. *Refer to EIA Standards 556 and 624*.

Figure 2 – Maximum Component Rotation

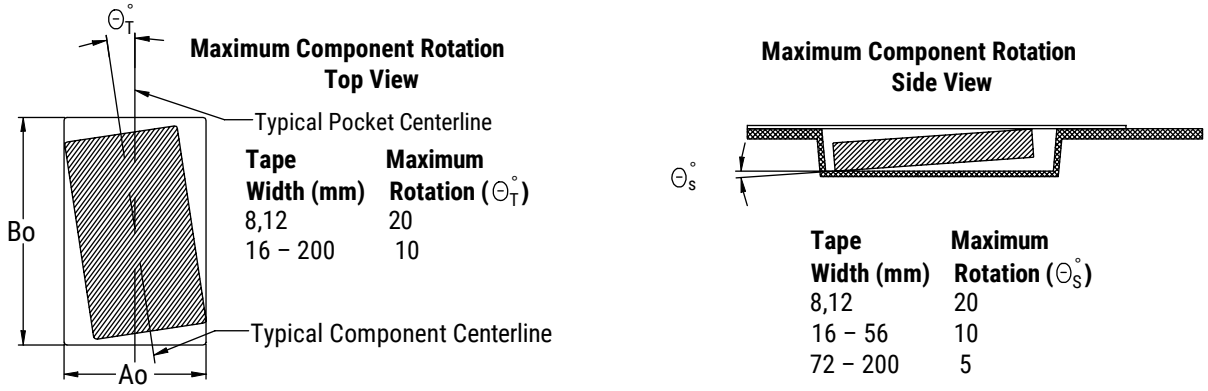


Figure 3 – Maximum Lateral Movement

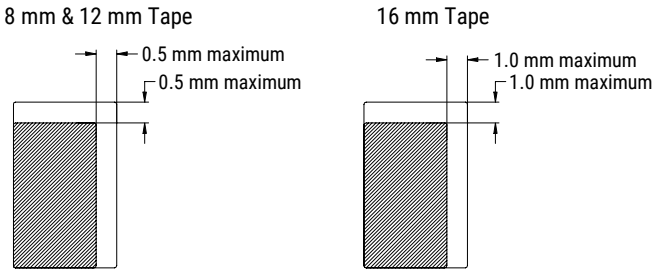


Figure 4 – Bending Radius

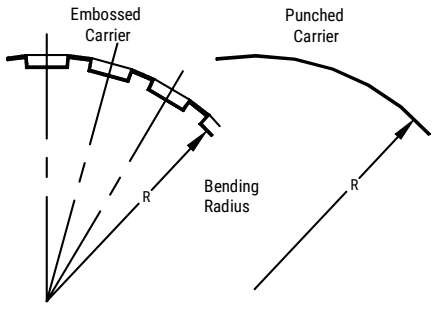
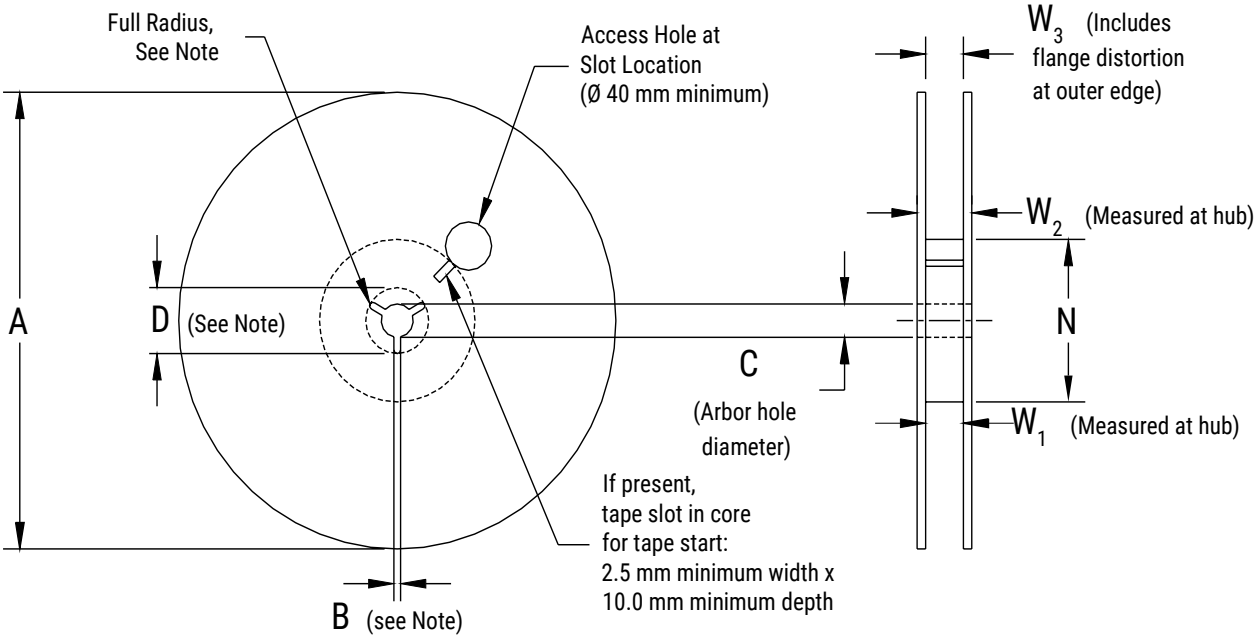


Figure 5 – Reel Dimensions



Note: Drive spokes optional; if used, dimensions B and D shall apply.

Table 7 – Reel Dimensions

Metric will govern

Constant Dimensions — Millimeters (Inches)				
Tape Size	A	B Minimum	C	D Minimum
8 mm	178 ±0.20 (7.008 ±0.008) or 330 ±0.20 (13.000 ±0.008)	1.5 (0.059)	13.0 +0.5/−0.2 (0.521 +0.02/−0.008)	20.2 (0.795)
12 mm				
16 mm				

Variable Dimensions — Millimeters (Inches)				
Tape Size	N Minimum	W_1	W_2 Maximum	W_3
8 mm	50 (1.969)	8.4 +1.5/−0.0 (0.331 +0.059/−0.0)	14.4 (0.567)	Shall accommodate tape width without interference
12 mm		12.4 +2.0/−0.0 (0.488 +0.078/−0.0)	18.4 (0.724)	
16 mm		16.4 +2.0/−0.0 (0.646 +0.078/−0.0)	22.4 (0.882)	

Figure 6 – Tape Leader & Trailer Dimensions

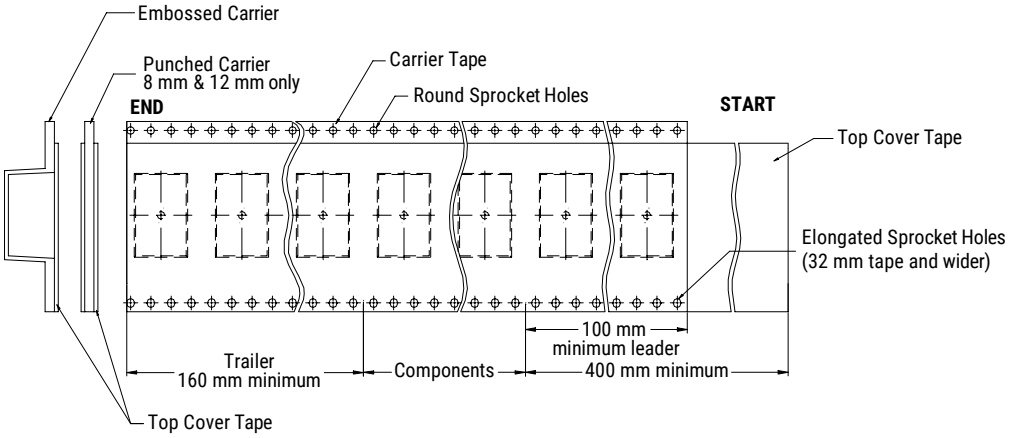
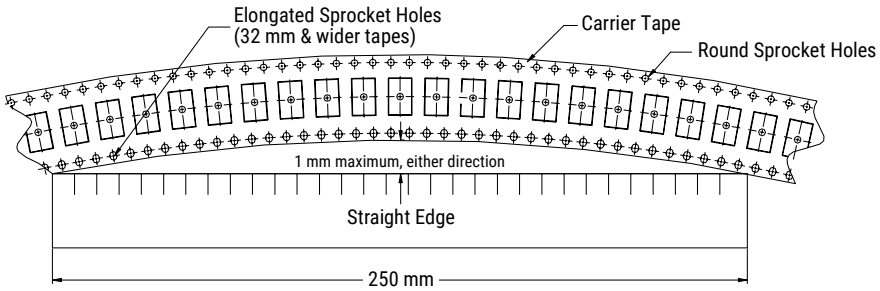


Figure 7 – Maximum Camber



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